Ku-band Low Noise MMIC Amplifier with Bias Circuit for Compensation of Temperature Dependence and Process Variation

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Abstract — **In this paper, a Ku-band Low-Noise MMIC amplifier is presented, which is equipped with a bias circuit that compensates not only temperature dependence of FETs' gain but also gain variation between chips due to process variations. The Ku-band low noise MMIC amplifier with proposed gate-bias circuit was designed and manufactured. It was proved that the proposed bias circuit reduced the temperature dependence of the two-stage MMIC amplifier's gain from 1.4 dB/100K to 1.0 dB/100K. The chip area consumed for the bias circuit is less than 10% of the total chip size of 1.17mm^2. The gain variation between chips was reduced to 0.25 dB in RMS. This amplifier is suitable for active phased array applications.**

I. INTRODUCTION

Recently, some active phased array antenna systems are proposed for commercial communication systems, e.g. LEO satellite communication systems [1,2], an airplane antenna system [3,4,5]. For commercial success, cost reduction is essential and cost of MMICs, which sometimes dominates the cost of Tx/Rx modules, should be reduced. Many works have been dedicated to realize miniature MMIC amplifiers for low cost [5,6,7].

For use in active phased array antennas, MMICs are requested to show small variation between chips to achieve stringent tracking requirements. Moreover, temperature dependence of MMICs are desired to be small because temperature in a whole antenna might vary in tens of degrees and large temperature dependence of MMICs might lead to serious beam tracking problems.

In addition to the efforts to minimize chip size of the MMICs, to make Tx/Rx module cost more reasonable, it is very important to eliminate any costs accompanying with MMIC installation, such as gain tuning using external substrates, external capacitors or inductors to suppress low frequency oscillations, and external circuits to compensate temperature dependence of the MMIC amplifiers. Self-biasing circuit is often used to suppress the effect of process variations [5,6]. However, it does function to maintain a constant drain current and might worsen temperature dependence of the MMIC amplifier in case the change in gain with respect to temperature is in opposite direction to that of drain current. The situation is sometimes true for the case of GaAs low noise MMIC amplifiers.

The easiest way to achieve temperature compensation within MMIC amplifiers is to control gate voltage against temperature so that the gain of the MMIC amplifiers are kept constant with respect to temperature by constituting a proper bias circuit in MMICs. Yamauchi et al proposed a very simple temperature compensation circuit for high power MMIC amplifiers that utilizes temperature dependence of threshold voltages of diodes [8].

In this paper, we have developed a new gate-bias circuit for low noise MMIC amplifiers, in which we employed another FET in addition to diodes for temperature compensation of amplifiers with shallow gate setting. We have designed and manufactured Ku-band low noise MMIC amplifier with proposed gate-bias circuit. It was proved that the new bias circuit compensates not only temperature dependence of the gain but also gain variation between chips due to process variations.

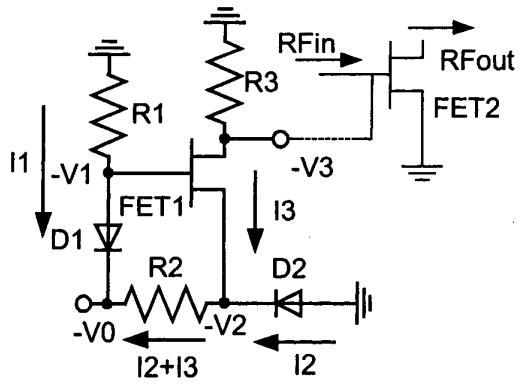

Fig. 1. The schematic diagram of the new gate-bias circuit proposed for simultaneous temperature compensation and process variation compensation. FET1 works only in DC mode. FET2 amplifies the microwave signals. All these components are to be integrated in a MMIC.

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II. Operation Principle

The schematic diagram of the proposed bias circuit is shown in Fig.1. Two diodes denoted by D1 and D2 are composed by short-circuiting the drain and source electrodes of FETs to integrate this bias circuit within a MMIC amplifier. FET1 is fabricated in the same process technology that the microwave amplifying FET (FET2) is.

A. Compensation of Temperature Dependence

The operation principle of the bias circuit shown in Fig.1 as a temperature dependence compensation circuit is as follows;

1) When the ambient temperature of the chip rises, the currents that flow through D1 & D2 become larger because threshold voltage of semiconductor Schottky diode shifts to smaller when ambient temperature rises.

2) The gate voltage of FET1 (=-V1) decreases (becomes larger in negative) while the source voltage of FET1 (= -V2) increases (becomes smaller in negative).

3) The current that goes through the FET1 (=I3) is suppressed because the gate-to-source voltage of FET1 (= -V1+V2) is decreased (becomes larger in negative).

4) The output voltage of the bias circuit (=-V3), which is fed to the gate electrode of the microwave amplifying FET (FET2), increases (becomes smaller in negative) because V3 is expressed as

$$V3 = I3\ R3 \qquad (1)$$

5) In general, the gains of the microwave amplifiers decrease as temperature increases and increase as drain currents increase. The increase of V3 with respect to the temperature increases the drain current of FET2, and hence compensates the decrease of gain of FET2.

The two diodes, one connected at the gate and the other connected at the source of FET1, double the change of I3 with respect to the temperature and enhance the temperature compensation effects.

FET1 is essential when we utilize the temperature dependence of threshold voltage of diode for temperature compensation of low noise MMIC amplifiers. The threshold voltages of GaAs Schottky diodes are about 0.7 ~ 0.8 V while typical gate bias for low noise HEMTs are about -0.1 ~ -0.3V. FET1 converts the change of the threshold voltages of (and currents flowing through) the diodes D1 and D2 to the change of the current flowing through FET1 (=I3). As the gate voltage for FET2 is given by (1), we can set almost arbitrary gate voltage ranging from MESFETs (e.g. Vg = -1 ~ -2 V) to low noise HEMTs (e.g. Vg = -0.1 ~ -0.3 V) by choosing appropriate R3 independent of the limitation of the threshold voltage of the diodes.

D2 also plays one more important role: When I3 is reduced in high temperature condition, the voltage drop at R2 might be also reduced because it is given by

$$-V2 + V0 = R2\ (I2 + I3) \qquad (2)$$

It would partially cancel the change of V2 and reduce the compensation effect. However, in practice, the current I2 which flow through D2 increases due to the nonlinear nature of diode D2 and such a situation is prevented.

B. Compensation of Process Variation

The operation principle of the bias circuit shown in Fig.1 as a process variation compensation circuit is as follows;

1) Assuming that the gate bias voltage that is required to set a given drain current of FET2 (say 10mA for Wg=200μm) slightly shifts to a lager value due to the process variation within a wafer or within a lot. The drain current would decrease if biased at a constant gate voltage.

2) The current that goes through FET1 (=I3) also decreases because FET1 and FET2 are formed closely within a small chip with all the same fabrication process.

3) As the gate voltage for FET2 is given by (1), the decrease of drain current will partially recovered and gain variation due to process variation will be also partially compensated.

Again, the nonlinearly of D2 plays an important role for process variation compensation.

III. Experimental

The proposed bias circuit has been implemented in a Ku-band two stage GaAs low noise MMIC amplifier. The chip view is shown in Fig. 2. It employs two AlGaAs/ InGaAs pHEMTs for low noise operation in Ku-band, whose gate length and gate width are 0.25μm and 200μm respectively, loaded with source inductors for simultaneous noise and gain matching. To achieve small chip size, spiral inductors are used for matching elements. The proposed bias circuit is comprised of two 50x2μm FETs as diodes, one 10x2μm FET and three resistors. Those gate widths were chosen to satisfy desired temperature compensation characteristics. The total chip size is as small as 1.08x1.08mm^2 and chip area shared for the bias circuit is less than 10% of it.

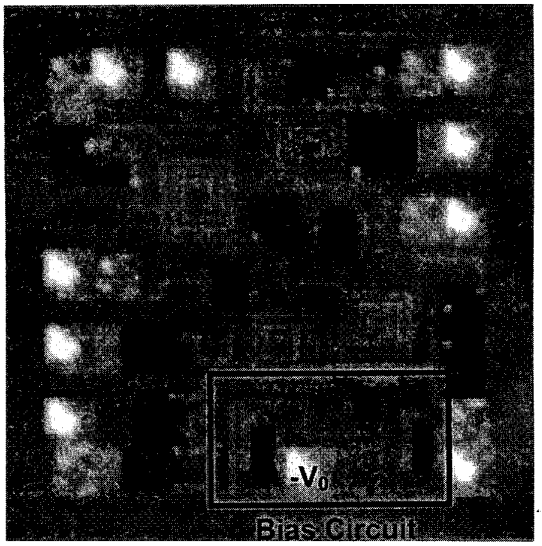

Fig. 2. The chip view of Ku-band low noise GaAs MMIC amplifier with the temperature and process variation compensation bias circuit. The chip dimension is 1.08mm x 1.08mm.

The nominal bias condition for this amplifier is Vd=3V and Id=20mA at room temperature. The S-parameters and noise figures of manufactured chips were evaluated on-wafer in the temperature ranging from –25degC to 75degC. The external bias voltage $-V_0$ was kept at a constant value of -1.2 V. Fig. 3 shows the measured S-parameters and noise figure of the amplifiers in the temperature range. The amplifier showed a gain of > 16dB, a noise figure of < 1.4dB• input and output return losses of > 15dB around DBS frequency (11.25 - 12.75GHz) at room temperature.

Fig. 4 shows the temperature dependencies of the gain at 12GHz and drain current of the amplifiers with and without proposed bias circuit. As we expected, the proposed bias circuit compensates the change of gain against temperature by changing the drain current. The temperature dependence of the gain at 12 GHz is reduced from 1.4dB/100K to 1.0dB/100K for the sake of the proposed bias circuit.

We also confirmed the compensation of process variation. About 100 same chips in a wafer were evaluated on condition that the external bias $-V_0$ is kept constant. The distribution of the gain at 12 GHz is shown in Fig 5 for (a):with and (b):without proposed bias circuit. The gain distribution at 12GHz were refined from 0.4dB RMS to 0.25 dB RMS by employing our new bias circuit.

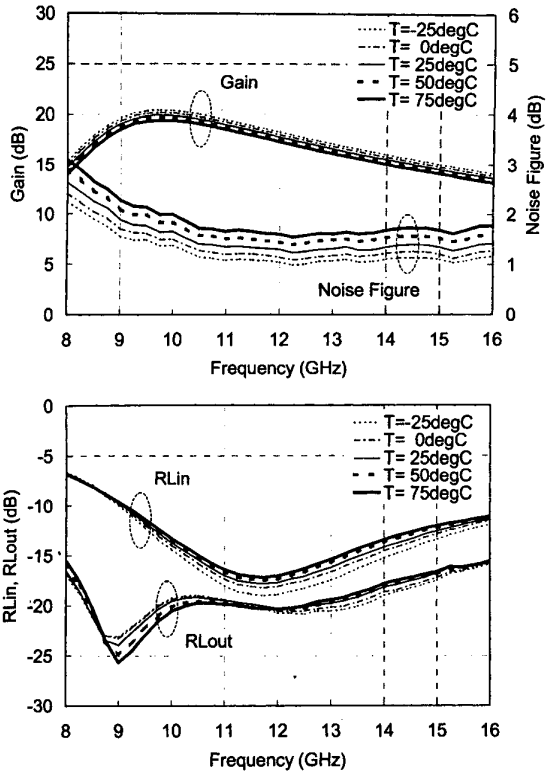

Fig. 3. Measured S-parameters and noise figure of the Ku-band low noise MMIC amplifier with proposed bias circuit. The external bias $-V_0$ was kept constant at which the drain current consumed in the chip is about 20mA at room temperature.

IV. Conclusion

In conclusion, we have developed a new gate-bias circuit embedded in a low noise MMIC amplifier which compensates not only temperature dependence of FETs' gain but also gain variation between chips due to process variations. A Ku-band low noise MMIC amplifier with proposed gate-bias circuit was designed and manufactured. The proposed bias circuit reduced the temperature dependence of the two-stage MMIC amplifier from 1.4dB/100K to 1.0dB/100K. and gain variation between chips from 0.4dB to 0.25dB in RMS. The chip area consumed for the bias circuit was less than 10% of the total chip size of 1.17mm^2. We conceive that this bias circuit will drastically reduce the total cost of active phased array antennas and contribute to their commercial success.

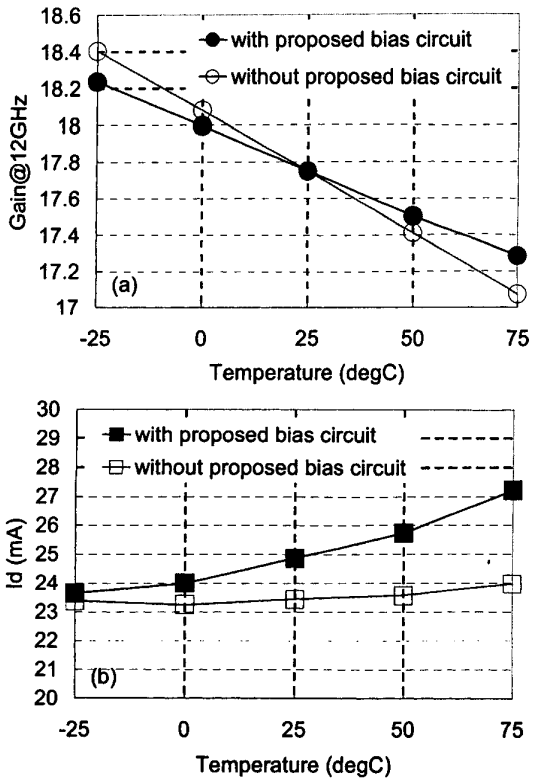

Fig. 4. Temperature dependencies of (a):gains at 12 GHz and (b):drain current consumed in chips for with (filled mark) and without (open mark) proposed bias circuit.

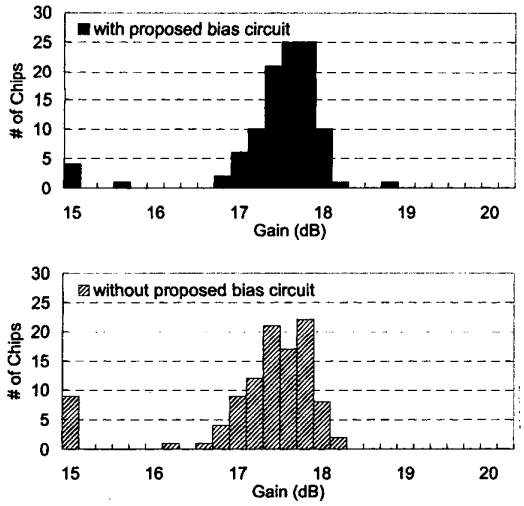

Fig. 5. Gain distribution of about 100 chips from a wafer. (a):with proposed bias circuit; (b):without proposed bias circuit (@12GHz).

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